22.7 6.33mW MPEG Audio Decoding on a Multimedia Processor

Yoshitaka Ueda[1], Hideki Yamauchi[1], Mamoru Mukuno[1], Shinji Furuichi[1], Mayumi Fujisawa[1], Fei Qiao[2], Huazhong Yang[2]

[1]SANYO Electric, Gifu, Japan
[2]Tsinghua University, Beijing, China

Techniques used to ensure low power usage are very important for battery-driven multimedia processors used in wireless or multimedia applications. However, the latest multimedia applications such as H.264/MPEG4/AAC/MP3 audio/video system [5] are computationally intensive placing ever greater demands on power consumption and forcing further innovation in low-power techniques.

Techniques to realize a low power multimedia application signal processor are presented, namely: (1) a parallel processing DSP for low voltage operation, (2) multi-power domains, and (3) a conditional pre-charge flip-flop. The combination of these low power techniques is able to reduce power dissipation without degrading operation speed and area, and uses only a single power supply. The techniques can reduce the power dissipation of the multimedia signal processor by 72.5% without area penalty or speed degradation. Furthermore, it allows the use of conventional CAD tools.

Figure 22.7.1 shows a block diagram of the multimedia application signal processor. It consists of a 32b RISC CPU with 160kB memory cache, a dedicated hardware DSP, USB2, DMA controller, Serial I/F, memory card I/F, timers, ADC, etc. The MPEG audio processes are carried out by using a dedicated hardware DSP which is comprised of hardwired functional blocks such as bit stream parsers, Huffman decoders, IQs, IMDCTs, synthesis filters, output formatter for DA, etc. All of the functions for audio processing are carried out by the hardwired functional blocks. Also in order to support multi audio standards (AAC/MP3/MPEG audio), individual functional blocks for multi-standards are integrated into the DSP. In addition, parallel and pipelined processing of each hardwired block is adopted in this hardware audio DSP. For instance, the Huffman decoder/IQ, IMDCT, and output formatter are pipelined. By making use of hardwired functional blocks and parallel and pipelined processing, the required operating frequency for MPEG decoding can be lowered to 30MHz. As a result, the voltage supply for MPEG decoding can be reduced to 1.1V from 1.8 and 1.3V, which is especially effective at reducing the dynamic power dissipation. The dynamic power is reduced by 62.7% as shown in Fig. 22.7.5.

To obtain the high bandwidth data flow necessary for multimedia signal processing, a multiple-bus architecture is applied as shown in Fig. 22.7.1. The multiple-bus is comprised of one high-speed bus and 3 peripheral buses. The main bus connects data transfer extensive blocks, such as the hardwired dedicated DSP, memory card IF, USB2 PHY, etc. The capacity of this bus is 288 MB/s. The peripheral buses connect serial ports, timers, ADC, etc. The capacity of this bus is 72 MB/s. With this multi-bus architecture, high-capacity data can be effectively transferred without causing any conflicts with slow data. External memories are connected via an external memory controller.

This processor has a multi power domain that is divided into 6 parts. Each part is connected to an individual 1.1V power supply that can be turned off. For example, in the case of AAC decoding, three power domains are turned off.

Figure 22.7.2 shows the circuit of the proposed conditional pre-charge flip-flop. In this circuit structure, the clock signal (CLK) is gated by the input signal (D, Db) so that there are only a minimum number of node changes even if data changes as shown in Fig. 22.7.3. With a conventional flip-flop, a lot of nodes change uniformly when the clock signal is toggled, and as a result, large power is dissipated. Therefore the proposed conditional pre-charged flip-flop can reduce the dynamic power dissipation associated with the clock signal compared with the conventional flip-flop.

In general, the power dissipation of the flip-flop consists of two parts: (1) the power dissipation owing to the transition of clock signal (CK) and, (2) the power dissipation owing to transition of the data signal (D). The proposed conditional pre-charged flip-flop can reduce the power dissipation owing to the transition of the clock signal by 95%. The power dissipation ratio is varied according to the data signal transition probability, as shown in Fig. 22.7.4. For example, with a 30% data signal transition probability, the power dissipation is reduced by 49.5% compared with a conventional flip-flop.

The previous low power conditional flip-flop [2][5] has a drawback of the long delay time from clock to output (Q and Qb). In the proposed conditional pre-charge flip-flop, the additional serial output circuit added to the output stage can improve the delay time from clock to output. The delay time is nearly the same as the conventional flop-flop and is 1/3 faster compared with a previous low power conditional flip-flop [2]. Figure 22.7.6 summarizes the performance of the proposed conditional pre-charged flip-flop.

The processor operates with a 1.1V supply using 0.15um CMOS technology. The 1.1V supply reduces the power dissipation, especially in the flip-flops, which comprise a dominant component of the power budget.

The developed multimedia signal processor consumes 6.33mW when it decodes MPEG audio. It can decrease the power dissipation by 72.5% compared with the conventional processor as shown in Fig. 22.7.5.

Figure 22.7.7 is a chip micrograph of the multimedia application processor. It is fabricated using a 6M 0.15μm CMOS process with chip dimensions of 6.6×6.7mm^2. It integrates 2.5M transistors.

Acknowledgements:
The authors wish to thank our team members, Mr. Isao Ogura, and Dr. Steve Yang for their contributions.

References:
[1] H. Kawaguchi, and T. Sakurai: "A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Clock Power Reduction," *Dig. Symp. on VLSI Circuits*, pp. 97-98, June, 1997.
[2] M. Hamada, et. al. "Flip-Flop Selection Technique for Power-Delay Trade-off," *ISSCC Dig. Tech. Papers*, pp. 270-271, Feb., 1999.
[3] Yan Zhang, Huazhong Yang, and Hui Wang, "Low clock-swing conditional-precharge flip-flop for more than 30% power reduction," *Electronics Letters*, vol. 36, no. 9, pp. 785-786, Apr., 2000.
[4] H. Yamauchi, et. al., "An 81MHz, 1280 × 720pixels × 30frames/s MPEG-4 Video/Audio Codec Processor," *ISSCC Dig. Tech. Papers*, pp.130-131, Feb., 2005.
[5] M. Hamada, et. al. "A conditional Clocking Flip-Flop for Low Power H.264/MPEG-4 Audio/Visual Codec LSI," *Proc. CICC*, pp. 527-530, Sept., 2005.

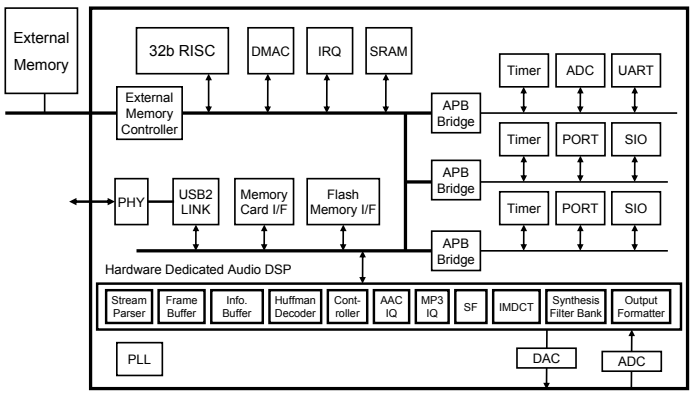

Figure 22.7.1: Block diagram of the developed SOC.

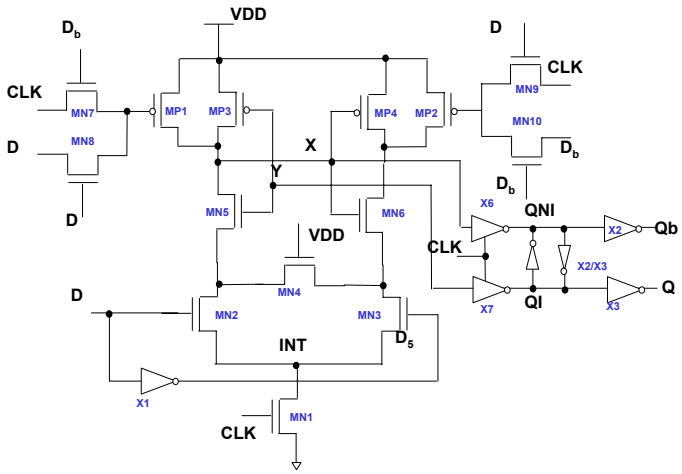

Figure 22.7.2: Circuit of the conditional pre-charged Flip-flop.

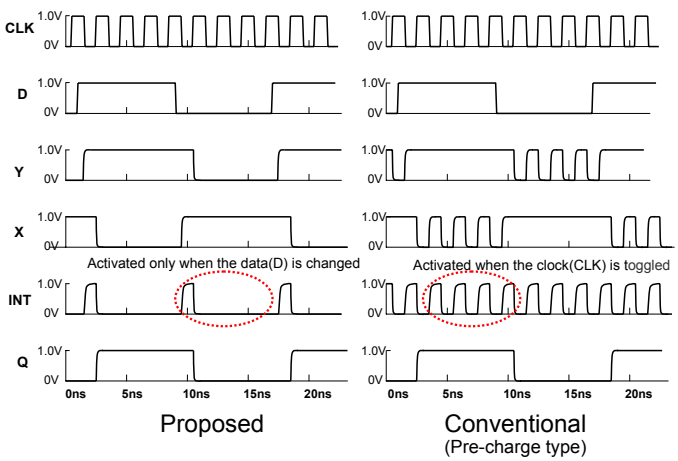

Figure 22.7.3: Operation of the conditional pre-charged Flip-flop.

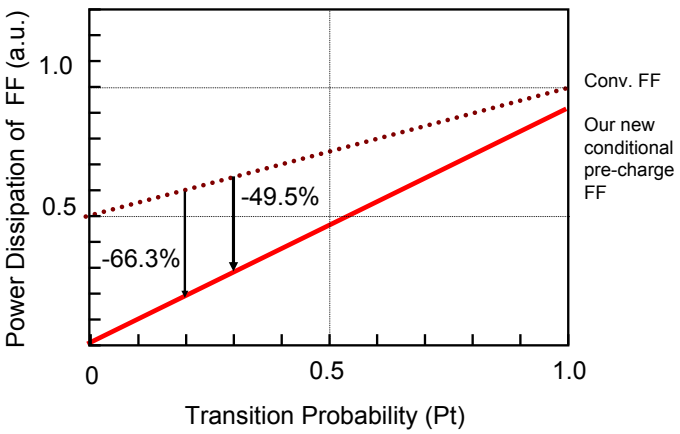

Figure 22.7.4: Comparison of the power dissipation.

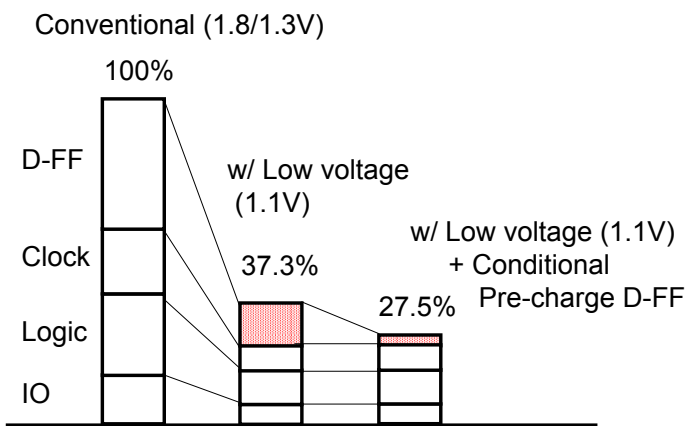

Figure 22.7.5: Power reduction of the SOC employing the proposed D-FF.

	Conventional D-FF	Previous Conventional Conditional D-FF	Proposed Conditional Pre-charge D-FF
Power [uW/MHz] (@Pt=0.3)	4.52 (1)	-- (0.5)	2.28 (0.504)
Delay [ps] (CK->Q + Setup)	351 (1)	-- (2.837)	345 (0.983)
Area [um^2]	41.13 (1)	-- (1)	41.13 (1)

Pt : Transition Probability

Figure 22.7.6: Comparison with previous works.

Continued on Page 662

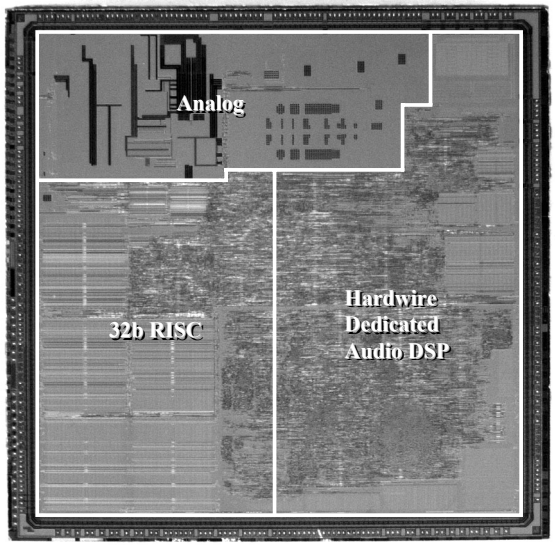

Figure 22.7.7: Chip micrograph.

